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Logarithmic Multiplier Using Seamless Pipelined

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Abstract: In a current scenario Logarithmic Number System (LNS) is the mostly used words in the field of arithmetic operations. In all arithmetic operations multiplication is most area/power/delay consuming component, but researchers have analyzed that, Logarithmic multiplier using seamless pipelined technique has potential to solve this problem. Hence, this paper gives a detailed and meaningful discussion of the seamless pipelined of LNS, systematic developments of the LNS multiplier architecture design, highlights the research areas, a further possibility of improvements.

Keywords: Arithmetic circuits, logarithmic multiplication, Mitchell method, Operand decomposition, Seamless pipelined.

1. Introduction

Arithmetic operations are the broadly used in the field of Digital signal processing (DSP), and image processing applications [1]. As, we know that Multiplication is most an area/delay/power consuming component of arithmetic operations. But LNS has potential to solve this problem [2-4]. LNS provide an option for fast computing. The signed logarithmic numbers has been kept in the defined format [5] [6]. The IEEE 754 standard sets formats for LNS: 1) Single precision 2) Double precision [7]. The logarithmic multiplication has mainly distributed in three steps: (1) conversion of binary numbers into the logarithmic numbers, (2) arithmetic operations are performed into the logarithmic domain, and (3) the antilogarithmic conversion of logarithmic numbers [4]. Now, the challenge is to make the multiplication efficient regarding hardware architecture as well as accuracy.

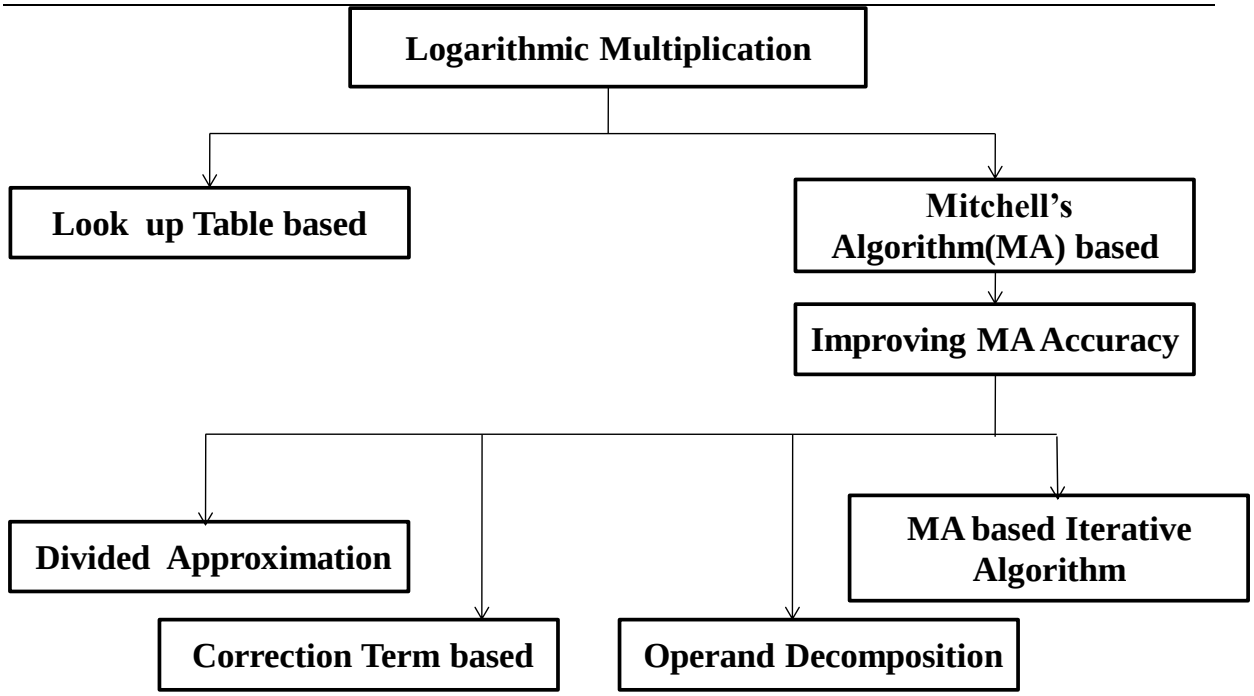
A simple example of multiplication of two logarithmic numbers 16 and 60 is given below [8].

Let A=b' (00010000) =d'16; and B=b' (00111100) =d'60;
Log A =0100.0000; and Log B=0101.11100;
Sum = Log A + Log B
Sum = (0100.0000) + (0101.11100) =1001.11100;
Antilog (Sum) = Antilog (Log A + Log B);
Antilog (Sum) =00000011110000000;
X*Y= Antilog (Sum) =960;

Rest of paper has been organized as the brief overview of LNS is described in Section 2. Proposed techniques of logarithmic multiplication have been explored further in Section 3. Section 4 gives synthesis and simulated results. And finally, explores the applications of LNS and the conclusion is concluded in Section 5.

2. Review of Logarithmic Multiplication Methods

Step by steps development of logarithm multiplication methods are given in the block diagram given in Fig. 1. LNS multipliers can be divided into two categories: (1) Look-Up Tables (LUT) and interpolations and (2) Mitchell's algorithm [3-10]. Mitchell's algorithm can be subdivided into four sub-categories namely as a) divided approximation b) correction based terms c) operand decomposition and d) MA-based iterative algorithm.



In 1962, Mitchell proposes an algorithm for multiplication and division [7]. Interpolation based LNS multiplier gives high accuracy, but due to hardware complexity the design cost becomes high. In 2003, Abed and Siferd developed correction algorithm that required trade-off between the accuracy, speed and complexity. Its three distinct corrections strategies based on equations for two, three and six regions with varying hardware complexity and accuracy. One of the hallmarks of Abed and Siferd, their study reduces the maximum percent errors that result from 0.9299 percent, 0.4314 percent and 0.1538 percent .In 2009 and 2011, Juang *et.al* propose a two region bit level manipulation scheme to achieve high accuracy with area, time and efficient hardware implementation [9]-[10]. It obviates the need of ROM circuits by using Boolean operations for the first four bits of the inputs. A similar approach has been used to achieve accuracy for an antilogarithmic converter. In 2015, Juang *et. al* 2 region logarithm approximation ranges over 0 to 0.0319 and ranges over -0.60 to 1.72 for antilogarithm converter [11].

The operand decomposition approach improves the average error percentage and the error range of Mitchell algorithms. It is equally applicable on all other methods like Divided Approximation based correction and correction term based methods [4]. The iterative logarithmic approximation is based on the correction terms, calculated immediately after the calculation of the product which avoids the comparison of the sum of mantissa with '1.' In this way, high-level of parallelism can be achieved by the principle of pipelining, thus the basic block for multiplication requires less logic resources and increasing the speed of the multiplier with error correction circuits[14]-[15].

3. Proposed Method

The existing approach does not provide a trade-off between the accuracy, and speed. We purpose a logarithmic multiplier using seamless pipelined to get further improvement in trade-off among various parameters.

3.1 Logarithmic multiplier using seamless pipelined

In this section, we understand the mathematical analysis of iterative algorithm with various possibilities for achieving an error as small as required and the possibility of achieving an exact result.

Consider two n-bit numbers N_1 and N_2 of the form.

$$X = x_{n-1}x_{n-2}.....x_2x_1x_0 \quad (1)$$

And

$$Y = y_{n-1}y_{n-2}.....y_2y_1y_0 \quad (2)$$

The final MA approximation for the multiplication depends on the carry bit form the sum of the mantissas and is given by:

$$P_{M.A} = 2^{k_1+k_2}(1 + x_1 + x_2).\ \text{where}\ x_1 + x_2 < 1 \quad (3)$$

$$P_{M.A} = 2^{1+k_1+k_2}(x_1 + x_2).\ \text{where}\ x_1 + x_2 \geq 1 \quad (4)$$

The binary representation of multiplication of two numbers N_1 and N_2 is express as below:

$$P_{true} = N_1 * N_2 = 2^{k_1+k_2}(1 + x_1 + x_2) + 2^{k_1+k_2}(x_1 x_2) \quad (5)$$

For avoid approximation error, we take.

$$x * 2^k = N - 2^k \quad (6)$$

Putting the value of equation (19) in equation (18) and we find.

$$P_{true} = N_1 * N_2 = 2^{(k_1+k_2)} + (N_1 - 2^{k_1})2^{k_2} + (N_2 - 2^{k_2})2^{k_1} + (N_1 - 2^{k_1}) * (N_2 - 2^{k_2}) \quad (7)$$

Suppose that

$$P^{(0)}_{approx} = 2^{(k_1+k_2)} + (N_1 - 2^{k_1})2^{k_2} + (N_2 - 2^{k_2})2^{k_1} \quad (8)$$

Is the first approximation of the product and P_{true} is the

$$P_{true} = P^{(0)}_{approx} + (N_1 - 2^{k_1}) * (N_2 - 2^{k_2}) \quad (9)$$

The absolute error after the first approximation is

$$E^{(0)} = P_{true} - P^{(0)}_{approx} = (N_1 - 2^{k_1}) * (N_2 - 2^{k_2}) \quad (10)$$

If we repeated multiplication procedure till n correction terms, we can approximate the product as:

$$P^{(n)}_{approx} = P^{(0)}_{approx} + \sum_{j=1}^{n} C^{(j)} \quad (11)$$

3.2. Functional Architecture of the Logarithmic multiplier using seamless pipelined

The general block diagram of the logarithmic multiplier using seamless pipelined is shown in Fig. 2. The computations consisting of six major blocks: leading one detector (LOD), priority encoder, barrel shifter (left), adder, decoder, and a seamless pipelined register.

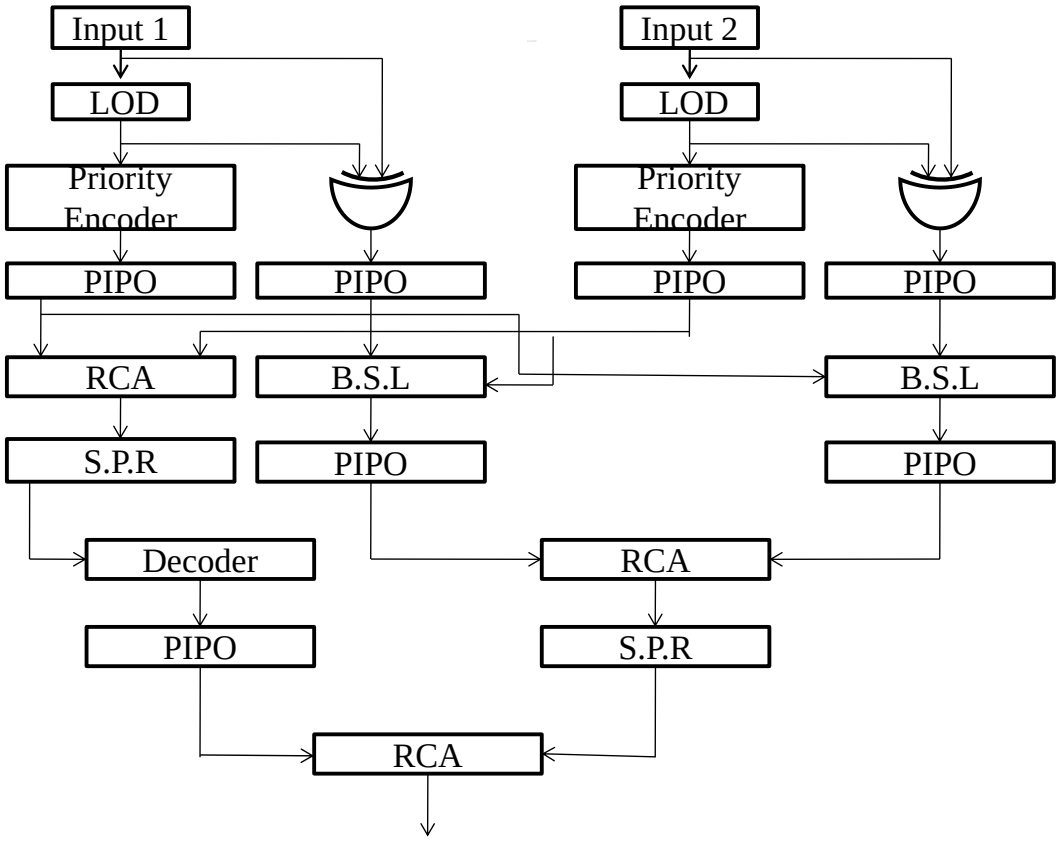


Fig.2. Block diagram of proposed seamless pipelined logarithmic multiplier

Here in fig.2 PIPO stands for parallel in parallel out register, RCA stands for ripple carry adder, BSL stands for barrel shift register, and SPR stands for seamless parallel register. Functionality of various blocks is discussed as: the LOD is simple to design and give result which count the position of LSB, priority encoder expand the LOD as a number, barrel shifter shift number in left side. Seamless pipelined is a newly proposed concept by Dr. Pramod Kumar Mehar, here this concept apply on this architecture at the suitable place of pipelining where it has possibility of apply, it reduced delay of architecture without any increment of area[16]. And finally we remove unnecessary and unremarked pipelined. We use component level hardware minimization also for improve hardware performance. As in the seamless pipelined implementation of the basic block the residues are available after the first stage. The correction circuit can now start to work immediately after the first stage from the prior block is finished. The seamless pipelined multiplier with one correction circuits is presented in figure 3.

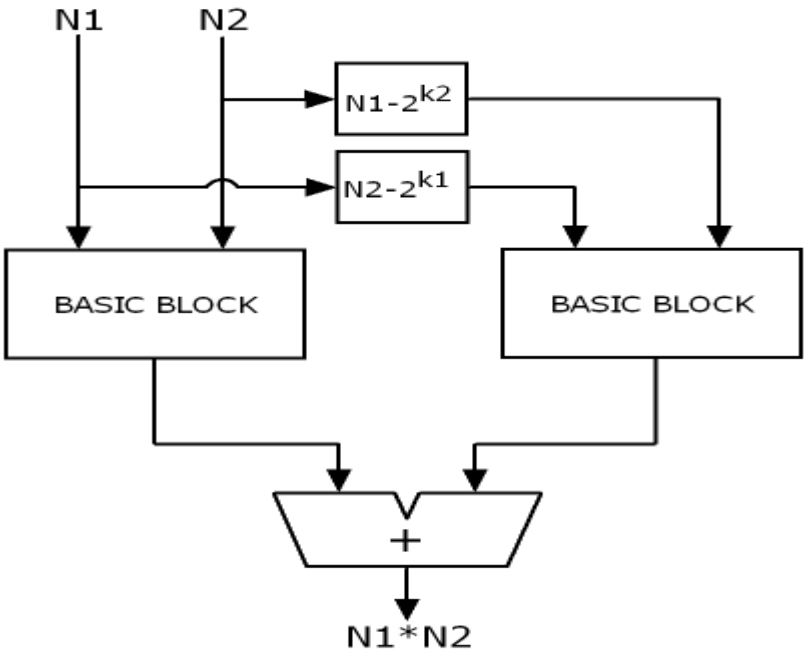


Fig.3. Block diagram of the proposed seamless pipelined multiplier with one error correction circuits

4. Results and Discussion

The proposed structure has N input samples and produces a 2N output sample Where N is equal number of bits used as the input bits .The proposed structure for logarithmic multiplication involves a leading one detector, XOR gate, priority encoder, barrel shift (left), RCA circuit, decoder circuit, PIPO register and seamless pipelined PIPO register.

4.1 Synthesis results

Our motive to suggest the seamless pipelined technique to construct a logarithmic multiplier architecture which is efficient in terms of the delay, power, and area. We concentrate to minimize the hardware with an equal accuracy. To fulfill this target we apply seamless pipelined register in place of simple pipelining.

We have synthesized the proposed logarithmic multiplier using seamless pipelined architecture by using at 90 nm CMOS technology node performance evaluations for 8, and 16 bits have been carried out. We have implemented and synthesizing the designs of the 8, and 16 bits a simple pipelined logarithmic multiplier of [14]. The area, power, and timing constraints are compared with the reported Logarithmic multiplication [14] with the seamless pipelined logarithmic multiplier, with the error correction circuit as listed in Tables 1. The ADP is defined as the amount of resources consumed by the hardware structure to provide unit throughput while EPS is defined as the power consumed by the hardware structure per unit throughput. The ADP and EPS for the proposed and reported structures [44] , are also listed in Tables 1.

Table1. Synthesis results of proposed Logarithmic Multiplication using seamless pipelined architecture and reported structures [14].

Structure	Existing[14]		Proposed	
	N=8	N=16	N=8	N=16
DAT(ns)	37.04	73.80	32.80	58.55
Area(μm^2)	9557.47	22381.69	8578.33	21619.27
Power(µW)	103.63	263.36	110.7	280.6
ADP(μm^2*µs)	354.008	281.369	165.176	126.580
EPS(n J)	3826.23	19435.968	3630.96	16429.13

As shown in Table 1, the proposed logarithmic multiplier using seamless pipelined architecture involve 11.45 % , and 20.67 % less DAT, 10.25 % and 3.41% area, 20.52 % and 23.37 % ADP, 5.12 %, and 15.47% less EPS for 8 bits, and 16 bits architecture respectively than of the reported A simple pipeline logarithmic multiplication structure [14].

5. Conclusion

Seamless pipeline can be reduced any circuits critical path better then pipeline techniques. Pipeline can only reduced DAT upto 10 % but Seamless pipeline reduced upto 20 % at same hardware cost sometimes hardware requirement is also less. Our main motive of design a hardware architecture of logarithmic multiplication is to make a efficient multiplier because in DSP applications where accuracy is not a big deal. We want less hardware resource required multiplier because binary multiplier takes lot of hardware resources. After implementation of logarithmic multiplication using seamless pipelined fulfill our motive. This multiplier is hardware efficient multiplier and capable to use everywhere as a component and independent multiplier.

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